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10/659,115	09/10/2003	Sun Hyoung Lee	DAE-0009	3574

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,115	LEE ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/10/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/10/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

- Claims 1-20 have been submitted for examination
- Claims 1-20 have been rejected

Claim Rejections - 35 USC § 112

1. Regarding claims 3, 8 and 16, the phrase "**substantially**" renders the claim indefinite because the applicant discloses the **same** SRAM-compatible structure of the memory bank(s) and the parity bank (Note FIG. 1, reference characters (10-0) and (12) in the applicant's drawings and page 6, lines (1-50 in the specifications). See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi et al. US publication no. 2003/0086306 (Hereinafter Takahashi).

3. In regard to claim 1, Takahashi teaches:

   - An SRAM-compatible memory including a plurality of memory banks each having a plurality of DRAM cells arranged in a matrix form defined by rows and columns, the DRAM cells

interfacing with an external system which does not provide a separate timing period for performing a refresh operation for the DRAM cells, comprising:

(Note: Section [0023], line 7, in Takahashi)

- the memory banks for receiving and storing input data externally provided, the memory banks generating bank information signals each indicating whether a corresponding memory bank is subjected to an invalid read-access;

(Note: Section [0010], lines (6-20) in Takahashi)

- a parity generator for receiving the input data to generate input parity, the input parity being determined base on the input data and a preset parity value;

(Note: FIG. 1, reference character (260) in Takahashi)

- a parity bank for storing the input panty' and generating a panty' information signal indicating whether the parity bank is subjected to the invalid read-access; and

(Note: FIG. 1, reference character (120) in Takahashi)

- a data corrector receiving the bank information signals and fetched data from the memory banks and generating output data having same value as the input data by correcting data fetched from a memory bank subjected to the invalid read-access if a checked parity value is different from the preset parity value, the checked parity value being obtained using the

fetched data provided from the memory banks and parity data fetched from the parity bank.

(Note: FIG. 1, reference characters (250) and (300) in Takahashi)

4. In regard to claim 2, Takahashi teaches:

- The SRAM-compatible memory according to claim 1, wherein the data corrector comprises:
- a bank data control unit for receiving the bank information signals and the fetched data to provide bank control data, any of the bank control data corresponding to fetched data provided from any of the memory banks subjected to the invalid read-access has a first logic value;

  (Note: FIG.1, reference characters (110), (160-1,2,3) and (130) in Takahashi)
- a parity data control unit for receiving the parity information signal and the parity data fetched from the parity bank to provide parity control data;

  (Note: FIG. 1, reference character (250) in Takahashi)
- a discriminating unit for receiving the bank control data and the parity control data and providing discrimination data having a second logic value contrary to the first logical value if the fetched parity data is different from the input parity; and

  (Note: FIG. 1, reference character (300) in Takahashi)

- a selecting unit for selecting the bank control data or the discrimination data in response to the bank information signals to generate the output data.

  (Note: FIG. 1, reference character (230), in Takahashi)

5. In reference to claim 3, Takahashi teaches:

   - The SRAM-compatible memory according to claim 2, wherein the panty' bank has a substantially same structure as each of the memory banks.

     (Note: FIG.2, reference characters (110) and (120) in Takahashi)

6. In regard to claim 4, Takahashi teaches:

   - The SRAM-compatible memory according to claim 2, wherein the memory banks each independently store corresponding one of the input data.

     (Note: FIG.2, reference character (110) in Takahashi)

7. In regard to claim 5, Takahashi teaches:

   - The SRAM-compatible memory according to claim 2, wherein each of the memory banks independently performs a read-access operation in response to a read command externally provided.

     (Note: Section [0025] in Takahashi)

8. In regard to claim 6, Takahashi teaches:

- The SRAM-compatible memory according to claim 2, wherein the refresh operation is independently performed with respect to the respective memory banks, and is prevented from being simultaneously performed with respect to two or more memory banks

  (Note: Sections [0041] and [0042] in Takahashi)

9. In regard to claim 7, Takahashi teaches:

- The SRAM-compatible memory according to claim 2, wherein:
- the bank data control unit includes a plurality of first logic devices each performing logic AND operation with respect to an inverted signal of corresponding one of the bank information signals and the fetched data provided from corresponding one of the memory banks to generate corresponding one of the bank control data; and

  (Note: FIG. 2 (Decoder 250) in Takahashi)
- the parity data control unit includes a second logic device performing logic AND operation with respect to an inverted signal of the parity information signal and the parity data to provide the parity control data.

  (Note: FIG. 2 (Decoder 250, E1 through E5) in Takahashi)

10. Claim 8 is rejected for the same reasons as per claim 3.

11. Claim 9 is rejected for the same reasons as per claim 4.

12. Claim 10 is rejected for the same reasons as per claim 5.

13. Claim 11 is rejected for the same reasons as per claim 6.

14. In regard to claim 12, Takahashi teaches:

- The SRAM-compatible memory according to claim 7, wherein the selecting unit includes a plurality of multiplexers each receiving corresponding one of the bank control data from corresponding one of the first logic devices and the discrimination data from the discriminating unit and selecting the corresponding one of the bank control data or the discrimination data in response to corresponding one of the bank information signals.

  (Note: FIG. 1, reference characters (230), (270) and (300) in Takahashi)

15. In regard to claim 13, Takahashi teaches:

- The SRAM-compatible memory according to claim 12, wherein the multiplexers each select the discrimination data when the corresponding one of the bank information signals indicates that the fetched data is provide from a memory bank subjected to the invalid read-access.

  (Note: Section [0010], lines (6-20) in Takahashi)

15. In regard to claim 14, Takahashi teaches:

- The SRAM-compatible memory according to claim 13, wherein the multiplexers each select the corresponding one of the bank

control data when the corresponding one of the bank information signals indicates that the fetched is valid.

(Note: FIG. 1, reference character (230), in Takahashi)

16. Claim 15 is rejected for the same reasons as per claim12.

17. Claim 16 is rejected for the same reasons as per claim 8.

18. Claim 17 is rejected for the same reasons as per claim 9.

19. In regard to claim 18, Takahashi teaches:

The SRAM-compatible memory according to claim 15, wherein each of the memory banks independently performs a read-access operation in response to a read command externally provided.

(Note: Section [0023], line 7, in Takahashi)

20. Claim 19 is rejected for the same reasons as per claim 11.

21. Claim 20 is rejected for the same reasons as per claim 1.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Leung et al. US publication no. 2005/0044467 teaches a memory system with transparent error correction.
- Leung et al. US publication no. 2003/0093744 teaches a memory device that uses error correction code (ECC).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

2/6/06

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